PCB DFM CHECKLIST

50 Common Design Mistakes That Kill Your First-Pass Yield

A practical, printable guide for PCB designers and engineers.
Check every item before submitting your Gerber files.

2,400+	18,000+	98%	15
Designs Reviewed	Issues Caught	First-Pass Yield	Years Experience

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PRO TIP: *Print this checklist and go through it item by item before submitting Gerber files. Each checkbox lets you confirm you've verified the design point. Items marked in red are critical — they cause the most costly production failures.*

SECTION 1 TRACE WIDTH & SPACING

8 checks for copper traces — the most common source of etching failures and signal integrity issues.

01 ☐ **Minimum trace width meets process capability**

Verify all traces meet the minimum width for your chosen copper weight. Thinner traces etch inconsistently and break.

```
Min: 4mil (1oz) | 5mil (2oz) | 8mil (3oz)
```

02 ☐ **Minimum trace spacing meets process capability**

Adjacent traces too close cause shorts from etch undercut. Check both same-net and different-net clearances.

```
Min spacing: 4mil (outer) | 3.5mil (inner)
```

03 ☐ **Trace width correct for current capacity**

Undersized traces cause hot spots, resistance loss, and potential trace burns under load.

```
Use IPC-2152 calculator. 1oz/10mil ~ 0.5A external
```

04 ☐ **Differential pair spacing consistent**

Inconsistent differential pair gaps cause impedance discontinuities and signal reflections.

```
Gap variation < 10% over entire trace length
```

05 ☐ **Trace-to-board-edge clearance sufficient**

Traces too close to board edge risk exposure after routing/V-scoring.

```
Min 0.25mm (V-score) | 0.15mm (routed edge)
```

06 ☐ **No acute angle traces (< 45 degrees)**

Acute trace angles create acid traps during etching, causing over-etch and open circuits.

```
All bends should be 45-degree chamfer or arc
```

07 ☐ **Neck-down areas checked for current path**

BGA fanout neck-downs often create current bottlenecks. Verify reduced-width sections can handle the current.

```
Neck-down length should be minimized
```

08 ☐ **Teardrops added at pad-to-trace connections**

Teardrops improve manufacturing yield by reinforcing the connection between traces and pads.

```
Required for via pads; recommended for all SMD pads
```

PRO TIP: *For high-speed designs (USB 3.0, PCIe, DDR4+), trace width and spacing directly affect impedance. Always provide your impedance requirements with the stackup — don't rely on the fab house guessing your intent.*

SECTION 2 VIA DESIGN

8 checks for vias — wrong via parameters cause drilling failures, shorts, and reliability issues.

09 ☐ **Via drill size meets minimum for board thickness**

Aspect ratio (board thickness / drill diameter) must stay within plating capability.

```
Max aspect ratio: 8:1 standard | 10:1 advanced | 12:1 HDI
```

10 ☐ **Via-to-via spacing above minimum**

Closely spaced vias risk drill breakout and etch bridging between annular rings.

```
Min via-to-via: 0.2mm (standard) | 0.15mm (HDI)
```

11 ☐ **Via-to-trace clearance verified**

Insufficient clearance causes shorts between via annular rings and adjacent traces.

```
Min clearance: 0.15mm from annular ring edge
```

12 ☐ **Via annular ring adequate**

Small annular rings from drill wander cause broken connections. Check pad size vs drill size.

```
Min annular ring: 0.1mm (standard) | 0.075mm (HDI)
```

13 ☐ **Via-in-pad design uses correct fill method**

Vias in SMD pads must be filled and plated over, or solder will wick down during reflow.

```
Specify: resin-filled + capped (IPC-4761 Type VII)
```

14 ☐ **Blind/buried via stackup is manufacturable**

Verify your blind/buried via pairs match a feasible sequential lamination stackup.

```
Provide clear drill chart with via type per layer pair
```

15 ☐ **Thermal relief on vias connected to planes**

Direct connections to copper planes create massive heat sinks that prevent proper soldering.

```
4-spoke thermal relief, 0.25mm spoke width typical
```

16 ☐ **Back-drill required for high-speed stub removal**

Via stubs on high-speed signals (>5Gbps) cause resonance and signal degradation.

```
Specify back-drill depth with 0.2mm tolerance margin
```

SECTION 3 SOLDER MASK & SILKSCREEN

8 checks for solder mask and silkscreen — mask errors are the #1 hidden cause of assembly defects.

17 ☐ **Solder mask opening size correct for all SMD pads**

Undersized openings cause solder bridging; oversized openings expose copper that oxidizes.

```
Standard expansion: 0.05mm per side (NSMD pads)
```

18 ☐ **Solder mask dam between fine-pitch pads**

Missing mask dams between QFP/QFN pads cause solder bridging during reflow.

```
Min mask dam: 0.1mm (LPI) | 0.075mm (advanced)
```

19 ☐ **BGA pad mask opening type specified**

SMD vs NSMD pad type affects BGA soldering. Most BGAs require NSMD for reliability.

```
NSMD: mask 0.05-0.075mm larger than pad per side
```

20 ☐ **Mask-defined pads not used where SMD-defined needed**

Mask-defined pads have larger tolerance and shouldn't be used for fine-pitch components.

```
Use SMD-defined (NSMD) for pitch < 0.5mm
```

21 ☐ **Solder mask clearance around test points**

Test points need exposed copper for probe contact. Verify mask opening covers the entire pad.

```
Min test point: 1.0mm pad with 0.9mm mask opening
```

22 ☐ **Silkscreen not overlapping exposed pads**

Silkscreen ink on solder pads prevents proper solder wetting and causes cold joints.

```
Min 0.15mm clearance between silk and mask opening
```

23 ☐ **Component reference designators readable**

Minimum text height and line width ensures designators survive printing and are legible for debug.

```
Min text: 0.8mm height, 0.15mm line width
```

24 ☐ **Polarity and pin 1 markers present**

Missing polarity marks cause wrong-orientation assembly. Check ICs, diodes, connectors, LEDs.

```
Verify: dot, bar, triangle, or key on all polarized parts
```

PRO TIP: *Solder mask issues are invisible in Gerber viewers but cause massive quality problems. Always request a solder mask layer review from your fab — it's the most under-checked layer.*

SECTION 4 PANELIZATION & BOARD OUTLINE

8 checks for panelization — bad panels can't run on SMT lines and waste material.

25 ☐ **Process rails included with correct width**

SMT machines clamp on process rails. Missing or narrow rails = board can't run on the line.

```
Min rail width: 5mm | 8mm recommended for wave solder
```

26 ☐ **Tooling holes present on process rails**

Machine pins locate the panel. Wrong size or position = placement accuracy loss.

```
3x tooling holes, 2.4mm dia (or per SMT machine spec)
```

27 ☐ **Fiducial marks present and correct**

Global and local fiducials are required for machine vision alignment.

```
Global: 2-3 marks on panel | Local: 2 marks per fine-pitch IC
```

28 ☐ **V-score lines don't cross component areas**

V-scoring creates stress. Components near V-score lines can crack during depaneling.

```
Min 1mm clearance from V-score to nearest component
```

29 ☐ **Tab routing / mouse-bite design correct**

Too few tabs = board falls off during assembly. Too many = hard to depanel cleanly.

```
3-5 tabs per sub-board, 0.5mm drill mouse-bite holes
```

30 ☐ **Panel utilization optimized for material waste**

Wrong panel orientation or array count wastes expensive laminate material.

```
Target > 80% utilization. Try rotating board 90 degrees.
```

31 ☐ **Board outline has no overlapping or open contours**

Open or self-intersecting board outlines cause CNC routing failures.

```
All outline segments must form a single closed path
```

32 ☐ **Board cutouts and slots dimensioned correctly**

Internal cutouts need minimum router bit clearance. Too-small features can't be routed.

```
Min slot width: 0.8mm | Min internal corner radius: 0.4mm
```

PRO TIP: *If you're not sure how to panelize, just send us the single-board Gerber — we'll design the optimal panel for free as part of our DFM review. Most customers save 15-30% on unit cost from better panelization alone.*

SECTION 5 COPPER BALANCE & PLANES

8 checks for copper distribution — imbalanced copper causes warping, etching defects, and signal issues.

33 ☐ **Copper fill percentage balanced across layers**
Asymmetric copper distribution causes board bowing/twisting during reflow.
`Target: < 20% difference between any two layers`

34 ☐ **Copper thieving / hatched fill added to sparse areas**
Large bare areas next to dense copper etch at different rates, causing width variation.
`Add copper thieving to areas with < 30% fill`

35 ☐ **Ground plane splits checked for return current paths**
Splits in reference planes force return currents to detour, creating EMI and signal integrity issues.
`No signal trace should cross a plane split on adjacent layer`

36 ☐ **Thermal relief pads used on inner plane connections**
Direct connections to planes cause soldering failures due to excessive heat dissipation.
`4-spoke thermal relief, min 0.25mm spoke width`

37 ☐ **Copper pour clearance from board edge**
Copper too close to the board edge gets exposed during routing, risking short circuits.
`Min 0.5mm copper-to-edge clearance (routed boards)`

38 ☐ **No isolated copper islands (floating copper)**
Unconnected copper fragments act as antennas, cause ESD issues, and may violate EMC requirements.
`Run DRC to remove all floating copper`

39 ☐ **Power plane clearances adequate for voltage**
High-voltage nets need larger clearances to planes to prevent arcing and creepage.
`IPC-2221: 0.25mm/100V for internal layers`

40 ☐ **Copper weight specified correctly per layer**
Incorrect copper weight callout leads to wrong trace impedance and current capacity.
`Specify each layer: 0.5oz (signal), 1oz (power), 2oz (heavy current)`

SECTION 6 STACKUP & IMPEDANCE

6 checks for stackup and controlled impedance — critical for high-speed and RF designs.

41 ☐ **Stackup structure specified (not just layer count)**
Just saying "4-layer" is not enough. Core/prepreg thicknesses directly affect impedance.
`Provide full stackup: material, thickness, Dk value per layer`

42 ☐ **Impedance targets defined with tolerance**
Uncontrolled impedance on high-speed nets causes reflections and timing failures.
`Typical: 50 ohm SE, 90-100 ohm diff | Tolerance: +/-10%`

43 ☐ **Signal layers adjacent to reference planes**
Signal layers without adjacent ground/power reference planes have uncontrolled impedance.
`Every signal layer must have a continuous reference plane on adjacent layer`

44 ☐ **Material type specified for high-frequency**
Standard FR-4 (Dk ~4.5) is lossy above 3GHz. High-speed designs need low-loss materials.
`FR-4: < 3GHz | Mid-loss: 3-10GHz | Rogers/Megtron: >10GHz`

45 ☐ **Board total thickness within tolerance**
Overall thickness affects connector fit, enclosure compatibility, and flex behavior.
`Standard: 1.6mm +/-10% | Specify if tight tolerance needed`

46 ☐ **Symmetrical stackup maintained**
Asymmetric stackups (different copper/dielectric above and below center) cause warpage.
`Mirror stackup around center line`

PRO TIP: *Always request a pre-production impedance simulation from your fab. They can adjust trace widths based on actual material lot data for much tighter impedance accuracy than what your EDA tool calculates with nominal values.*

SECTION 7 ASSEMBLY (DFA) CONSIDERATIONS

4 checks that bridge PCB design and SMT assembly — often missed by layout engineers.

47 ☐ **Component spacing meets pick-and-place minimum**
Components too close together can't be placed by nozzles and create shadowing during reflow.
`Min 0.5mm between components (0.3mm for passives)`

48 ☐ **Pad footprints match component datasheets**
Wrong pad dimensions cause tombstoning (passives) or insufficient solder joints (ICs).
`Use IPC-7351 standard footprints as baseline`

49 ☐ **All SMD components on same side (if possible)**

Double-sided SMD requires two reflow passes, doubling cost and adding thermal stress risk.

```
Heavy components on top; light passives can go on bottom
```

50 ☐ **Assembly drawing and BOM synchronized**

Mismatches between BOM, schematic, and assembly drawing cause wrong-part placement.

```
Cross-check: part count, ref-des list, DNP markings
```

APPENDIX QUICK REFERENCE — KEY PARAMETERS

Print this page and keep it at your desk for fast lookups during PCB layout.

PARAMETER	STANDARD	ADVANCED	HDI
Min trace width	4 mil / 0.1mm	3 mil / 0.075mm	2 mil / 0.05mm
Min trace spacing	4 mil / 0.1mm	3 mil / 0.075mm	2 mil / 0.05mm
Min via drill	0.3mm	0.2mm	0.1mm (laser)
Min via pad	0.5mm	0.35mm	0.25mm
Min annular ring	0.1mm	0.075mm	0.05mm
Max aspect ratio	8:1	10:1	12:1
Min mask dam	0.1mm	0.08mm	0.06mm
Min mask expansion	0.05mm/side	0.04mm/side	0.03mm/side
Min silk text height	0.8mm	0.6mm	0.5mm
Min silk line width	0.15mm	0.12mm	0.1mm
Copper-to-edge	0.5mm	0.3mm	0.25mm
Min slot width	0.8mm	0.6mm	0.5mm
Panel rail width	5mm	5mm	5mm
Tooling hole dia	2.4mm	2.4mm	2.0mm

PRO TIP: *These are general guidelines. Your specific fab house may have tighter or looser capabilities. Always confirm with your manufacturer before finalizing the design. Or better yet — send us your Gerber files at info@queenems.com for a free review and we'll check everything for you.*

Ready for a professional DFM review?

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